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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				Application Number	Not assigned yet
				Filing Date	On even date herewith
				First Named Inventor	J. YUGAMI, et al.
				Art Unit	Not assigned yet
				Examiner Name	Not assigned yet
Sheet	1	of	1	Attorney Docket Number	520.40885VX1

U.S. PATENT DOCUMENTS						
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)				
SG		6.495.890	B1	12-2002	Ono	
SG		5.514.891		05-1996	Abrokwa et al.	

FOREIGN PATENT DOCUMENTS							
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>2</sup> -Number <sup>3</sup> -Kind Code <sup>4</sup> (if known)					
SG		JP	110003990	1/6/99			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS				
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published		T <sup>2</sup>
SG		1998 International Electron Device Meeting Technical Digest, (Pgs. 1038-1040), A 1.1 nm Oxide Equivalent Gate Insulator Formed Using TiO <sub>2</sub> on Nitrided Silicon.		
SG		IEEE Transactions on Electron Devices, Vol. 46, No. 7, July 1999, (Pages 1537-1544), The Impact of High-k Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET's		

Examiner Signature	<i>And D. By</i>	Date Considered	7-20-04
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